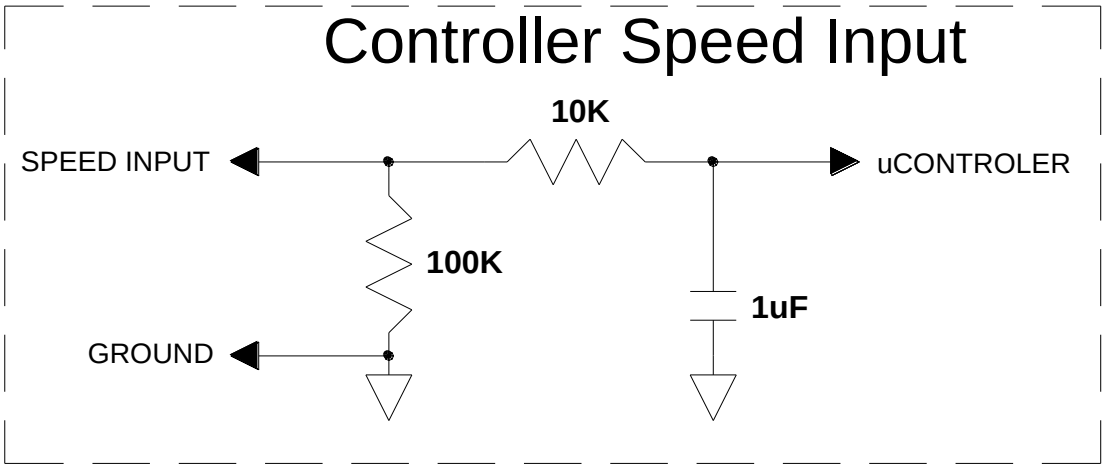
MASTERFLUX

Tips on applying PWM signal to the analog speed input.

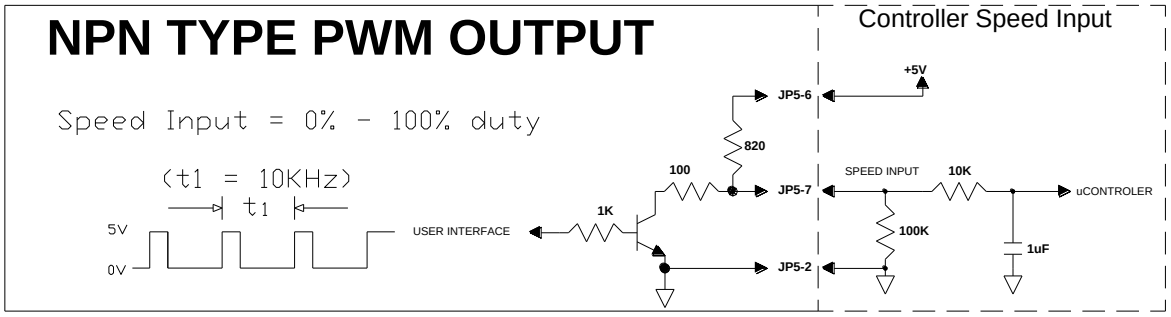
Summary / Overview
This document gives a brief overview of applying PWM signal to the 0-5V analog speed input. The analog input shown below has a low pass filter (100 Hz) that consists of 10K and 1uF used to filter the speed input. A 100K pull down resistor is in place for any leakage current in the circuit.

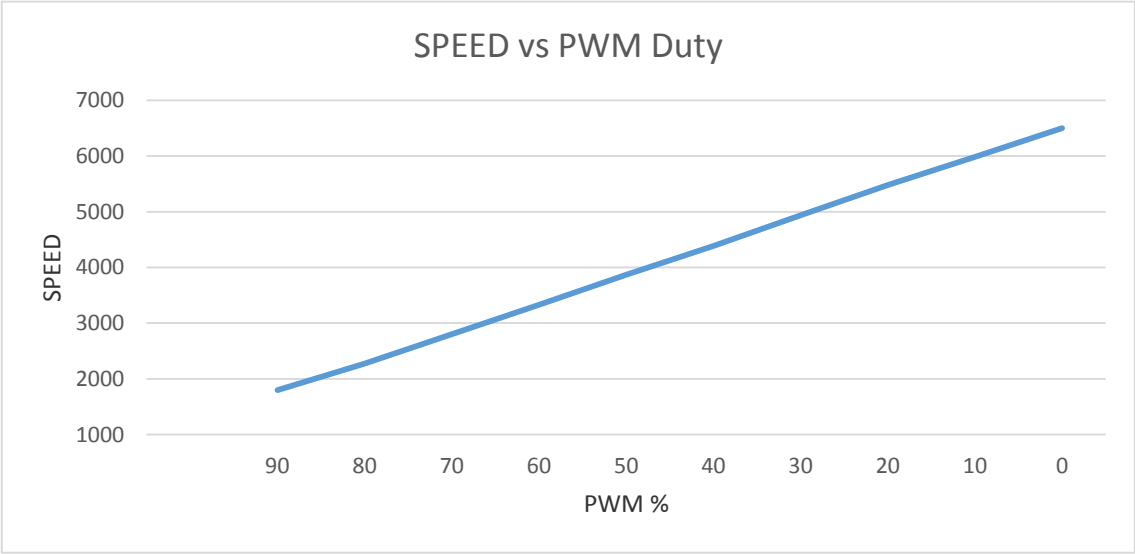
A minimum carrier frequency of 10 KHz is recommended to reduce the amount of ripple voltage at the speed input.

NOTE: The maximum voltage applied to the speed input must not exceed +5VDC.

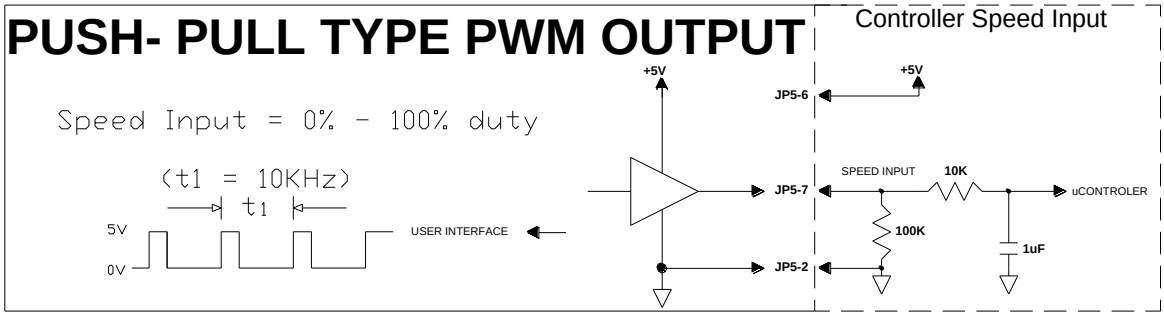


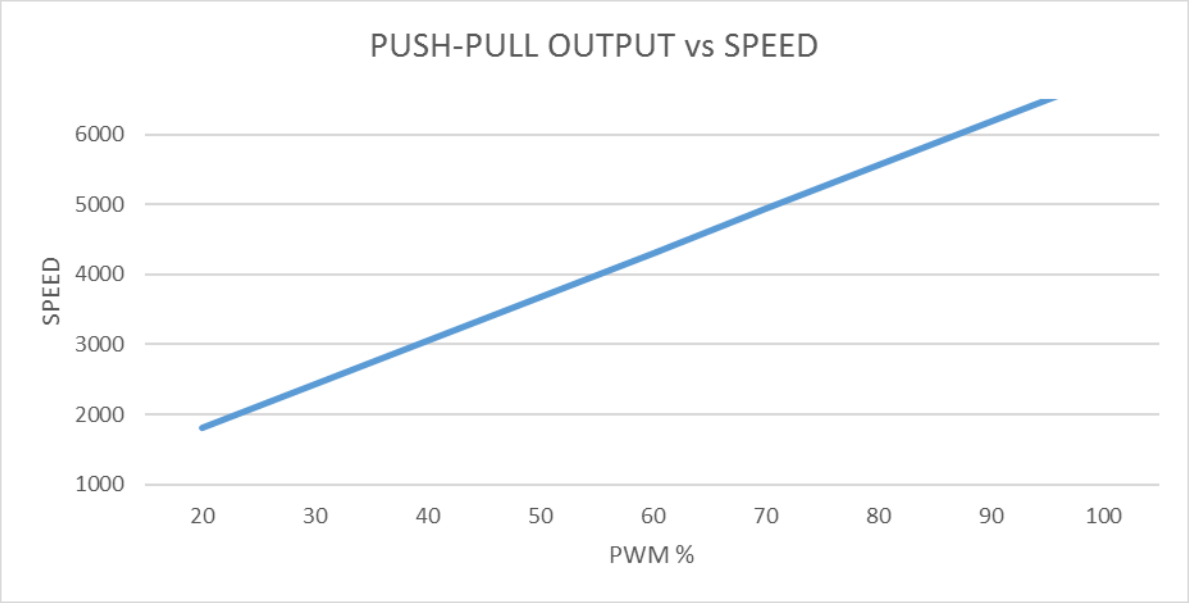
Below is a typical application where the PWM driver is an open collector NPN type transistor referenced to ground. In this scenario the interface requires an external pull-up resistor to the internal +5V that is brought out JP5 pin 6. An external series resistor is also required to limit the discharge rate. This also limits the minimum voltage that can be achieved when the PWM is at 100%.
With this configuration the PWM duty to speed is inverted due to the NPN transistor. See the speed to PWM duty chart below.





The diagram below uses a push-pull type driver where the output is driven active high and low. A resistor divider may be used to limit the input voltage at the speed input to +5VDC. The speed vs PWM table is below.





JP5 Pin function	
1	N.C.
2	GROUND
3	ON/OFF CONTORL
4	+VM (on/off control)
5	TACHOMETER OUTPUT
6	+5V OUTPUT (50mA max)
7	ANALOG SPEED INPUT
8	FAULT OUTPUT